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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/410,606	10/01/1999	DAVID ALAN EDWARDS	99-TK-239	7114

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EXAMINER	
MASKULINSKI, MICHAEL C	
ART UNIT	**PAPER NUMBER**
2184	20

DATE MAILED: 12/03/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/410,606	EDWARDS ET AL.
	Examiner	Art Unit
	Michael C Maskulinski	2184

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 October 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-36* is/are pending in the application.

4a) Of the above claim(s) *2,3,5,10,13,14,16,21,24,25,27 and 32* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4,6-9,11,12,15,17-20,22,23,26,28-31 and 33-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

Final Office Action

Claim Rejections - 35 USC § 103

1. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

2. Claims 1, 9, 12, 20, 23, and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Razban, U.S. Patent 5,289,587, and further in view of Swoboda, U.S. Patent 5,828,824.

Referring to claims 1, 12, and 23:

a. In column 2, lines 39-62, Razban discloses in-circuit emulation by providing a microprocessor's (at least one processor) program counter external to the device on a dedicated bus (a system bus/communication link coupling the processor and debug circuit). An emulator (a debug circuit) can then readily generate a list of executed instruction addresses by simply monitoring the bus. However, Razban doesn't explicitly disclose that the processor and debug circuit are implemented on a same integrated circuit. In column 9, lines 8-15, Swoboda discloses a CPU core debug facility (components of microcomputer implemented on the same integrated circuit). Further, in column 7, lines 25-29, Swoboda discloses that built in debug facilities provide both stop mode and real-time debug environments. It would have been obvious to one of ordinary skill at the time of the invention to include the implementation of components of the microcomputer operating in real time on the same integrated circuit of Swoboda into the system of Razban. A person of ordinary skill in the art would have been

motivated to make the modification because *real-time debug facilities insulate time critical (interrupt driven) portions from debug activity* (see Swoboda: column 7, lines 35-37).

b. In column 4, lines 28-34, Razban discloses that the program counter register contains the virtual address of the first byte of the instruction currently being executed by the microprocessor. The address value contained in the program counter is incremented to point to the next instruction only when the microprocessor completes execution of the current instruction. Therefore, the program counter has a value corresponding to a value of the program counter at a writeback stage of a pipeline of the processor.

c. In column 4, lines 53-61, Razban discloses that if an exception occurs during execution of an instruction (indicating the status of computer instruction), the microprocessor will trap via its conventional trap mechanism.

Referring to claims 9, 20, and 31:

a. In column 2, lines 39-62, Razban discloses in-circuit emulation by providing a microprocessor's (at least one processor) program counter external to the device on a dedicated bus (a system bus/communication link coupling the processor and debug circuit). An emulator (a debug circuit) can then readily generate a list of executed instruction addresses by simply monitoring the bus. However, Razban doesn't explicitly disclose that the processor and debug circuit are implemented on a same integrated circuit. In column 9, lines 8-15, Swoboda discloses a CPU core debug facility (components of microcomputer implemented

on the same integrated circuit). Further, in column 7, lines 25-29, Swoboda discloses that built in debug facilities provide both stop mode and real-time debug environments. It would have been obvious to one of ordinary skill at the time of the invention to include the implementation of components of the microcomputer operating in real time on the same integrated circuit of Swoboda into the system of Razban. A person of ordinary skill in the art would have been motivated to make the modification because *real-time debug facilities insulate time critical (interrupt driven) portions from debug activity* (see Swoboda: column 7, lines 35-37).

b. In column 2, lines 39-62, Razban discloses transmitting a program counter to an emulator for debugging purposes (the debug circuit is adapted to generate trace information including the program counter).

3. Claims 4, 15, and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Razban, U.S. Patent 5,289,587 and Swoboda, U.S. Patent 5,828,824, and further in view of Levine et al., U.S. Patent 5,862,371.

Referring to claims 4, 15, and 26, in column 2, lines 39-62, Razban discloses in-circuit emulation by providing a microprocessor's (at least one processor) program counter external to the device on a dedicated bus (a system bus coupling the processor and debug circuit). An emulator (a debug circuit) can then readily generate a list of executed instruction addresses by simply monitoring the bus. However, neither Razban nor Swoboda explicitly disclose indicating that the computer instruction is a first instruction past a branch instruction. In column 3, lines 41-55, Levine et al. disclose an

indication of whether or not a branch instruction was taken or not taken. Indicating that a branch was taken indicates that the next instruction is a first instruction past a branch instruction because the instruction after the branch was taken is found at the address in memory that it is branched to. It would have been obvious to one of ordinary skill at the time of the invention to include the branch indication of Levine et al into the system of Razban and Swoboda. A person of ordinary skill in the art would have been motivated to make the modification because *performance projections for processor systems and memory subsystems are important for a correct understanding of work loads within the system. An instruction trace is generally utilized to determine distribution of instructions, identification of register dependencies, branch path analyses and timing* (see Levine et al.: column 3, lines 28-33).

4. Claims 6-8, 17-19, 28-30, and 34-36 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Razban, U.S. Patent 5,289,587, and Swoboda, U.S. Patent 5,828,824, and further in view of Mann, U.S. Patent 6,314,530.

Referring to claims 6, 17, and 28, in column 2, lines 39-62, Razban discloses transmitting a program counter to an emulator for debugging purposes. However, neither Razban nor Swoboda explicitly disclose transmitting a process identifier value. In column 21, lines 3-51, Mann discloses tracing multi-tasking operating systems through the use of task ID's (process identifier value). It would have been obvious to one of ordinary skill at the time of the invention to include the task identification information of Mann into the combined debug system of Razban and Swoboda. A person of ordinary skill in the art would have been motivated to make the modification

because in a typical system multiple tasks or processes are running at the same time (a pipeline). *In order to know which task is now being traced, the operating system examines the task control block and writes some content (e.g., the task ID) from the task control block into the trace memory to identify the task or thread* (see Mann: column 21, lines 39-44).

Referring to claims 7, 18, and 29, in column 21, lines 34-51, Mann discloses that an operating system can identify an application task or thread switch in the trace memory by entering a code into a user defined TCODE indicating the task ID or thread ID that is being switched to or that was switched from (signal indicating that a current process identifier value differs from a processor identifier value of a previously-executed instruction).

Referring to claims 8, 19, 30, 34, 35, and 36, in column 4, lines 8-28, Mann discloses that the trace memory (memory-mapped register) has a plurality of locations for storing trace information that indicates execution flow of a plurality of instructions in the processor (program counter).

5. Claims 11, 22, and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Razban, U.S. Patent 5,289,587, and Swoboda, U.S. Patent 5,828,824, and further in view of Flynn, U.S. Patent 5,642,479. In column 2, lines 39-62, Razban discloses providing a microprocessor's program counter value external to the system. However, neither Razban nor Swoboda explicitly disclose transmitting a value indicating an amount by which the program counter is incremented. In column 1, lines 49-54, Flynn discloses a trace address increment signal generating

means for generating a trace address increment signal upon said trace bus. It would have been obvious to one of ordinary skill at the time of the invention to include the increment signal of Flynn into the combined debugging system of Razban and Swoboda. A person of ordinary skill in the art would have been motivated to make the modification because *the provision of a trace address increment signal enables a narrower trace bus to be used. Such a signal, which may be a single bit, is all that is required* (see Flynn: column 2, lines 9-14). Further, in column 5, lines 41-67 continued in column 6, lines 1-2, Flynn discloses signals that indicate the trace is sequential and can be incremented (incrementing the program counter by a value depending upon a mode signal).

Response to Arguments

6. Applicant's arguments filed October 3, 2003 have been fully considered but they are not persuasive.

7. On pages 14-17, under section 2.3 of the Applicant's remarks with respect to claims 1, 12, and 23, the Applicant argues, "Razban and Swoboda do not teach or suggest a microcomputer comprising, *inter alia*, at least one processor, wherein the at least one processor is configured to transmit to the debug circuit a status indicating that a computer instruction in the writeback stage is a valid computer instruction." Further, the Applicant argues, "Trapping an instruction if an exception occurs is not the same as transmitting to a debug circuit a status indicating that a computer instruction in the writeback stage is a valid computer instruction. In the system of Razban an exception may occur when executing an instruction, but there is no disclosure of a processor

transmitting to a debug circuit a status indicating that a computer instruction in the writeback stage is a valid computer instruction." The Examiner respectfully disagrees. In column 4, lines 53-61, Razban discloses a trap routine that is executed after an exception occurs. Entering into a trap routine provides a status of the computer instruction and having an exception occur is an indication that the computer instruction is not valid.

8. On pages 17-19, under section 2.3 of the Applicant's remarks with respect to claims 9, 20, and 31, the Applicant argues, "Neither Razban, Swoboda, or teach or suggest a microprocessor comprising, *inter alia*, at least one processor and a debug circuit, wherein the debug circuit includes means for generating trace information including the program counter." The Examiner respectfully disagrees. In column 2, lines 39-62, Razban discloses transmitting a program counter to an emulator for debugging purposes (the debug circuit is adapted to generate trace information including the program counter).

Conclusion

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael C Maskulinski whose telephone number is (703) 308-6674. The examiner can normally be reached on Monday-Friday 9:30-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert W Beausoliel can be reached on (703) 305-9713. The fax phone number for the organization where this application or proceeding is assigned is (703) 746-7239.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

MM

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